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DE: Taylor - ACM Computing Surveys (CSUR), 2005 - portal.acm.org  
 ... 2003]. Sev- eral algorithms in this class are amenable to high-performance **hardware** implemen-  
 tation. ... Page 8. Survey and Taxonomy of **Packet Classification** Techniques ...  $I=1$  b i (1) 1 We are  
 assuming a 32-bit address where an addi- tional 32 bits are used to specify a **mask**. ...

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P Gupta, N McKeown - Proceedings of the conference on Applications, ..., 1999 - portal.acm.org  
 ... Another recent proposal [15] describes a scheme optimized for implementation in **hardware**. ... Phase  
 0 Phase 1 Phase 2 Phase 3 Recursive **Classification** Figure 4: Showing the basic idea of  
 Recursive Flow ... Phase 0 Phase 1 Phase 2 Phase 3 Figure 5: The **packet** flow in RFC. ...

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K Lakshminarayanan, A Rangarajan. S ... - Proceedings of the 2005 ..., 2005 - portal.acm.org  
 ... describe some metrics for comparing algorithms used in the **packet classification** subsystem for ...  
 to append the search key with the appropriate bits, the **packet** processor needs ... TCAM modifications  
 to accommodate range matching better— such as **implementing** comparators at ...

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... The sequence of accesses made by the example **packet** have also been shown ... 148  
 Figure 4.30 An example **hardware** design for RFC with three phases. ... The leaf nodes  
 store a maximum of birth **classification** rules.....163 Figure ...

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A Kennedy, Z Liu, X Wang, B Liu - doi.ieeecomputersociety.org

... 5 when only 1 **classification** engine is used. The sorter logic block and multiplexers used for  
 multiplexing the output signals of the **classification** engines are not needed. IV. FPGA  
 IMPLEMENTATION We **implement** the multi-engine **packet** classifier using VHDL on a Stratix ...

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P Gupta - HOT INTERCONNECTS - eeweb1.poly.edu

... packets into flows (**packet classification**) Page 11. 11 Routing Lookups ... Harder than Exact Match ...  
 The destination address of an arriving **packet** does not carry with it the information to determine  
 the ... Cache management overhead >**Hardware** implementation difficult Page 40. 40 ...

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DE: Taylor, EW Spitznagel - Dept. Comp. Sci. Eng., Washington Univ., Saint ..., 2005 - Citeseer

... The seminal Parallel Bit-Vectors (BV) scheme used a simple bit-vector intersection technique  
 that maps well to **hardware** [5]. The presorting of filters by priority and poor ... The result is a  
 high-performance **packet classification** technique that is practical to **implement** that has ...

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V Sahasranaman, M Buddhikot - Proceedings of IEEE International ..., 2001 - bell-labs.com

... **2.2 Packet Classification** using Recursive Space-decomposition (PACARS) ... algorithm, we implemented search lists at each node as skiplists [6] and did not **implement** the fractional ... this set of potential tuples by hashing bits of the source and destination address of the packet. ...

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CR Meiners, AX Liu, E Torng - ... State University, Technical Report MSU-CSE ..., 2009 - cs.msu.edu

... To **implement** bit weaving, we must solve several challenging technical problems. ... TCAM-based **packet classification** systems have been widely deployed due to their  $O(1)$  classification time ... array for a possibly incomplete rule list (ie, there may exist at least one **packet** that none ...

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T Heinz - net.t-labs.tu-berlin.de

... **Hardware** algorithms: This class of algorithms is implemented in dedicated **hardware** devices attacking PCP by massive parallelism ... match is reduced to at most  $2k-i$  because each part of the **mask** match, corresponding ... The **packet classification** problem can be defined as follows ...

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